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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte VENKAT RANGAN, EDWARD D. McCLANAHAN, and
MICHAEL B. SCHMITZ

Appeal 2009-005288
Application 10/695,408
Technology Center 2100

Decided: December 11, 2009

Before HOWARD B. BLANKENSHIP, JOHN A. JEFFERY, and STEPHEN C. SIU, *Administrative Patent Judges*.

SIU, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

This is a decision on appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-36. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

Invention

The invention relates to a storage application platform for use in storage area networks (Spec. 2, ¶ [0004]).

Independent claim 19 is illustrative:

> 19. A network comprising:
>
> at least one host adapted to be connected to a switched fabric;
>
> at least two storage units, each adapted to be connected to a switched fabric; and
>
> a switched fabric connected to and coupling the at least one host and the at least two storage units, the switched fabric comprising:
>
> at least one switch for coupling to the at least one host and the at least two storage units; and
>
> a storage processing device coupled to the at least one switch and for coupling to the at least one host and first and second storage units of the at least two storage units, where the first and second storage units may be directly connected to the storage processing device or may be coupled through the at least one switch, the storage processing device to migrate data between the first and second storage units whether the first and second storage units are directly connected to the storage processing device or are coupled through the at least one switch, the storage processing device including:
>
> an input/output module including processors to receive, operate on and transmit network traffic; and

a control module coupled to said input/output module, said input/output module and said control module being configured to interactively perform data migration between the first and second storage units.

Reference

The Examiner relies upon the following reference as evidence in support of the rejection:

Testardi	US 2003/0140210 A1	Jul. 24, 2003

Rejection

Claims 1-36 are rejected under 35 U.S.C. § 102(e) as being anticipated by Testardi.

ISSUE 1

Appellants argue that "Testardi indicates that the storage units must be directly connected to the storage processing device" (App. Br. 12).

Issue: Did Appellants demonstrate that the Examiner erred in finding that Testardi teaches that the storage processing device may have the units directly connected or coupled through an external switch and that the data migration is performed in either case?

ISSUE 2

Appellants argue that instead of delaying the write operation, the fast path in Testardi "simply passes the operation on to the control path" (App. Br. 13).

Issue: Did Appellants demonstrate that the Examiner erred in finding that Testardi teaches delay of data write operations by the claimed processors?

FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

1. Testardi teaches that

> the data storage system 12 may also include switching fabric 20 which may include one or more switches and other associated hardware and software in connection with facilitating data transmissions between each of the host computer systems and the physical devices

(¶ [0062]; fig. 4a).

2. Testardi depicts physical devices 22a and 22b connected to fast paths and control paths within distributed virtualization engine 34a through switching fabric 20 (fig. 4a). This is shown by the placement of the physical devices outside the optional switching fabric boundary (¶ [0062]; fig. 4a).

3. Testardi teaches that "a switch may connect the FP1-1 [fast path] hardware and/or software implementation to physical device [2]2a" (¶ [0069]; fig. 4a).

4. Appellants admit that the fast path in Testardi "passes the [write] operation on to the control path" (App. Br. 13).

5. Testardi teaches that

> [i]f an FP [fast path] is able to dispatch the I/O [input/output] operation further to a particular physical device using a mapping table which is populated by the CP [control path] in this example, the FP does such dispatching without further intervention by the CP. Otherwise, the I/O operation may be forwarded to the CP for processing operations.

(¶ [0074]).

PRINCIPLES OF LAW

Claim interpretation

"In the patentability context, claims are to be given their broadest reasonable interpretations. . . . [L]imitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993) (citations omitted)

Anticipation

In rejecting claims under 35 U.S.C. § 102, "[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation." *Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375 (Fed. Cir. 2005) (citation omitted).

ANALYSIS

Issue 1

Based on Appellants' arguments in the Appeal Brief, we will decide the appeal with respect to issue 1 on the basis of claim 19 alone. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Testardi teaches that physical devices can be connected to components of a distributed virtualization engine through an optional switching fabric (FF 1, 2). Testardi also specifies that a switch may connect a fast path to a physical device (FF 3). It is inconsequential whether "Figs. 4B and 4C show the storage units directly connected to the switch 43" (Reply Br. 4) given that figure 4A, and its description, teach storage units that may be connected through a switch (FF 1-3). Therefore, Appellants are mistaken in their position that "storage units . . . connected through a switch goes against the express teachings of Testardi" (App. Br. 12).

Furthermore, Appellants have provided no arguments or evidence showing that Testardi's data migration operations would not be successful when the storage units are connected to the storage processing device through a switch.

For at least these reasons, we find that Appellants have not sustained the requisite burden on appeal in providing arguments or evidence persuasive of error in the Examiner's 35 U.S.C. § 102(e) rejection of claim 19, or of claims 1-18 and 20-36, which fall therewith, with respect to this issue.

Issue 2

Based on Appellants' arguments in the Appeal Brief, we will decide the appeal with respect to issue 2 on the basis of claim 3 alone. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Testardi teaches that when a fast path is unable to dispatch an input/output (i.e., write) operation, the fast path forwards the operation to the control path for processing (FF 5). This comports with Appellants' admission that the fast path in Testardi passes write operations on to the control path (FF 4).

Appellants argue that these teachings do "not meet the positive requirements in the claim that the processors perform the delaying operation" (App. Br. 13). However, claim 3 merely requires that "said processors delay data write operations" (claim 3; App. Br. 16) and does not specify the manner of effecting the delay. Moreover, Appellants do not dispute the Examiner's finding that passing the operation on to the control path delays the write operations (Ans. 8-9).

For at least these reasons, we find that Appellants have not sustained the requisite burden on appeal in providing arguments or evidence persuasive of error in the Examiner's 35 U.S.C. § 102(e) rejection of claim 3, or of claims 12, 17, 18, 21, 26, 27, 30, 35, and 36, which fall therewith, with respect to this issue.

CONCLUSIONS OF LAW

Based on the findings of facts and analysis above, we conclude that Appellants have not demonstrated:

1. that the Examiner erred in finding that Testardi teaches that the storage processing device may have the units directly connected or coupled through an external switch and that the data migration is performed in either case (Issue 1); and

2. that the Examiner erred in finding that Testardi teaches delay of data write operations by the claimed processors (Issue 2).

DECISION

We affirm the Examiner's decision rejecting claims 1-36 under 35 U.S.C. § 102(e).

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

msc

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